Patent Claims:

1. Analyzing device for an embedded system (9), which comprises at least one CPU (1), optionally at least one CPU bus (2), and at least one memory (3), including at least one communication module (4) for the input or output of analysis data using a test interface (5), c h a r a c t e r i z e d in that the test interface, in addition to control lines, includes at least one group of data lines transmitting data words and address words alternately or in other succession, and the information whether data words or address words are transmitted is transmitted by way of at least one control line so that the content and access operations during the operation time to the describable internal memory as well as I/O access operations of the embedded system can be monitored and/or logged practically without using basic cycles of the CPU (1).

2. Analyzing device as claimed in claim 1, c h a r a c t e r i z e d by two, in particular at least three, freely selectable analysis modes, with the analysis modes differing from each other in the way and extent of participation of the CPU 1 in reading and/or writing data for analysis purposes, and wherein depending on the selected analysis mode either

- all write access operations of the CPU to especially definable address ranges are logged without using basic cycles, or

- all read access operations of the CPU are logged, or
- direct reading and writing of the CPU from/into an external memory (6) is executed by using basic cycles.

3. Analyzing device as claimed in claim 1 or 2, c h a r a c t e r i z e d in that the communication module comprises a logic 22, 23 which independently has access to data and/or control and/or address information through a data connection in order to follow write and/or read access operations in real time, i.e. without CPU influencing.

4. Analyzing device as claimed in at least any one of claims 1 to 3, c h a r a c t e r i z e d in that the communication module is connected to a cache (8, 8', 8'') or especially comprises it, and data transmitted in write and/or read access operations can be stored in the cache, and in particular data out of the cache can be output in a buffered manner through the test interface (5) or data can be written into the cache using this interface, respectively.

5. Analyzing device as claimed in at least any one of claims 1 to 4, c h a r a c t e r i z e d in that the test interface (5) is connected to a test memory (6) arranged outside the embedded system, and the external test memory (6) is especially a central core memory or a dual-port memory.

6. Analyzing device as claimed in at least any one of claims 1 to 5,
c h a r a c t e r i z e d in that the data transmission from the communication module to the external memory takes place through a parallel interface (5).

7. Analyzing device as claimed in at least any one of claims 1 to 6,
c h a r a c t e r i z e d in that the external memory (6) is connected to a data conditioning device (7) which provides an interface connection (14) for external debugging applications.

8. Use of the analyzing device as claimed in at least any one of claims 1 to 7 in an embedded system which comprises a fully operable microcomputer with at least central processing unit (1) and data memory (3).

9. Use of the analyzing device as claimed in at least any one of claims 1 to 7 in an integrated microprocessor system for motor vehicles with at least two processor cores (15, 16), wherein a complete analyzing device (18), in particular as claimed in at least any one of claims 1 to 7, is associated with at least one of the processor cores (16) contained therein.

10. Use as claimed in claim 9,
c h a r a c t e r i z e d in that in addition to the first processor core (16) with the complete analyzing device, an incomplete analyzing device (17) is associated with another processor core (15) in the

integrated microprocessor system, having a reduced scope of functions compared to the complete analyzing device (18).

11. Use as claimed in claim 1 or 10,
c h a r a c t e r i z e d in that the reduction of the scope of functions involves that the cache (8' 8'') provided in the analyzing device has a small number of memory locations and/or a small word width, and/or the test interface (5) is not led to the outside, and/or the test interface (5) does not exist.

12. Method for the analysis of an embedded system with a test interface, in particular as claimed in at least any one of claims 1 to 7,
c h a r a c t e r i z e d in that for the transmission of data through the test interface, a data transmission protocol is used in which data is transmitted in several groups of addresses and data.

13. Method as claimed in claim 12,
c h a r a c t e r i z e d in that at least one mode is provided in which the analysis data in real time can be read out of the system which comprises at least CPU, data memory, program memory, and I/O element(s), and/or can be written into the system, so that the system need not be stopped or interrupted for the analysis.

14. Method as claimed in claim 12 or 13,
c h a r a c t e r i z e d in that
- the memory content or a correspondingly assessable information of the embedded system is copied in real

time completely or partly into an external memory, with the data being buffered in particular before the action, and/or

- the memory content of an external memory (6) or any correspondingly assessable information about the memory content of memory (6) is copied in real time completely or partly into a memory of the embedded system, with the data being buffered in particular before the action.

15. Method as claimed in at least any one of claims 12 to 14,
c h a r a c t e r i z e d in that only data necessary for debugging is transmitted to the external memory (6) in the event of access operations of the CPU to RAM 3.

16. Method as claimed in at least any one of claims 12 to 15,
c h a r a c t e r i z e d in that write access operations and/or read access operations of the CPU are logged by means of a cache (8, 8', 8'').

17. Method as claimed in at least any one of claims 12 to 16,
c h a r a c t e r i z e d in that information about the write access operations are written into the cache (8, 8', 8'') without additional CPU commands or directly into the communication module (4), and information about the read access operations is written into the cache with active assistance of the CPU.